Sub B1

a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and

a1

a compare register to compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

Sub B1

9. (Amended) A memory component with built-in self test, comprising:

a memory array;

an input/output interface coupled to the memory array and having a loopback;

a2

a controller to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array; and

a compare register to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

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a3 Sub B1

16. (Amended) A method of testing a memory component with built-in self test, comprising:

transmitting input/output test data to an input/output interface having a loopback;

receiving the input/output test data from the loopback of the input/output interface; and

comparing the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

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24. (Amended) A method of testing a memory component with built-in self test, comprising:

transmitting memory array test data to a memory array;

storing the memory array test data in the memory array

reading the memory array test data from the memory array; and

comparing the memory array test data transmitted to the memory array with the memory array test data read from the memory array, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

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31. (Amended) A memory module with built-in self test, comprising:

a plurality of memory components;

an address and command buffer adapted to transmit address and command data and test data to one of the plurality of memory components,

wherein the address and command buffer includes a register to receive a test result; and

at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from the one of the plurality of memory components to generate the test result, wherein the plurality of memory components, the address and command buffer, and the at least one data buffer all reside within the memory module.

39. (Amended) A method of testing a memory module with built-in self test, the method comprising:

transmitting address and command data and test data to a memory component among a plurality of memory components from an address and command buffer, wherein the plurality of memory components and the address and command buffer all reside within the memory module;

receiving the test data from the address and command buffer;

receiving the test data from the memory component; and

comparing the test data received from the address and command buffer with the test data received from the memory component to generate a test result.

48. (Amended) A memory module with built-in self test, comprising:

a plurality of memory components;

an address and command buffer adapted to transmit address and command data and test data to one of the plurality of memory components, wherein the address and command buffer includes,

a register to receive a test result,

a clock multiplier to receive a clock signal and to multiply the clock signal for transmission, and

an address and command generator to generate the address and command data; and

at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from the one of the plurality of memory components to generate the test result, wherein the plurality of memory components, the address and command buffer, and the at least one data buffer all reside within the memory module.